WHAT IS CLAIMED IS:

1. A SOI substrate comprising:

a SOI layer in which a device is to be formed; and

a supporting substrate wafer for supporting said SOI layer, said SOI layer and said supporting substrate wafer having been bonded to each other with an insulation layer interposed therebetween, in which

said insulation layer includes a cavity.

2. A SOI substrate in accordance with claim 1, in which said cavity is formed in a plurality of locations in a plane of said bonded SOI substrate.

3. A SOI substrate in accordance with claim 1 or 2, in which said insulation layer has a plurality of cavities defined by different heights.

4. A SOI substrate in accordance with claim 1, in which said SOI layer has varied thickness in the plane thereof.

5. A manufacturing method of a SOI substrate, comprising

a recessed portion forming step for forming a recessed portion in a surface of an active layer wafer and/or in a surface of a supporting substrate wafer;

a bonding step for bonding said active layer wafer and said supporting substrate wafer to each other with said surface(s) having said recessed portion(s) formed therein serving as bonding surface(s) to thereby form a cavity; and

a thinning step for thinning said active layer wafer of said bonded wafers to thereby form a SOI layer.

6. A manufacturing method of a bonded SOI substrate in accordance with claim 5, in which in said recessed portion forming step, said cavity is formed in a plurality of locations in said surface of said active layer wafer and/or in said surface of said supporting substrate wafer.

7. A manufacturing method of a bonded SOI substrate in accordance with claim 5 or 6, in which in said recessed portion forming step, a plurality of recessed portions having varied depth is formed in said surface of said active layer wafer and/or in said surface of said supporting substrate wafer.

8. A manufacturing method of a bonded SOI substrate in accordance with any one of claim 5 through 7, in which in said bonding step, an insulation film has been formed on said bonding surface of said active layer wafer and/or on said bonding surface of said supporting substrate wafer.

9. A manufacturing method of a bonded SOI substrate in accordance with claim 5, in which said bonding step is carried out in a vacuum atmosphere or under a vacuum condition.

10. A manufacturing method of a bonded SOI substrate in accordance with claim 5, in which said thinning step includes a step for grinding and polishing of said active layer wafer after having been bonded together.

11. A manufacturing method of a bonded SOI substrate in accordance with claim 5, further comprising a step for performing an ion implantation to a location in a specified depth in said active layer wafer, wherein said thinning step includes, in the course of a heat treatment

following to said bonding step, a step for separating a surface side of said active layer wafer from said ion-implanted region.

12. A semiconductor device comprising a bonded SOI substrate in which a SOI layer having varied thickness is formed over a plane thereof, wherein a functional block defined by a CMOS logic is formed in the thinnest region of said SOI layer and a memory functional block and/or an analog block are formed in the other regions of said SOI layer.

13. A semiconductor device in accordance with claim 12, in which a basic unit block of the CMOS logic is formed in the thinnest region of said SOI layer.

14. A semiconductor device in accordance with claim 13, in which a unit transistor is formed in the thinnest region of said SOI layer.

15. A semiconductor device in accordance with claim 14, in which a channel of a unit transistor is formed in the thinnest region of said SOI layer.